SIGNAL
Bulletin mensuel des microsystèmes
Microsystems Monthly Newsletter
RESMIQ
Regroupement Stratégique en Microsystèmes du Québec

FROM THE EXECUTIVE COMMITTEE

We are pleased to bring to your attention the activities of our center and the successes of its members for the month of February 2012. Firstly, regarding our regular activities, we held our first networking meeting of the year on February 2nd bringing to the forefront the work of our members at the University of Quebec at Montreal. This activity has enabled to connect researchers and industry representatives and was a success considering the presence of forty participants. We are already planning our next meeting to be held at Concordia University on March 15th. Also, to honor Prof. Hamoui, who passed away last November, his colleagues from ReSMiQ announce the establishment of the Anas Hamoui Scholarship. The terms of this competition will be posted shortly on the ReSMiQ's website. As for scientific activities, our annual symposium will be organized again as part of the upcoming 2012 ACFAS conference and will be held at the Palais des Congrès in Montréal on May 7. Finally, note that our Center will celebrate its 25th anniversary this summer. This is a major milestone that we will highlight significantly by measuring our progress since a group or researchers in the field of VLSI design obtained a five year grant. We invite you to participate in these events and looking forward for a large audience.

Best regards,
M. Sawan, director

Welcoming remarks by M. Mario Morin, Dean of the faculty of science of UQAM, at the ReSMiQ networking meeting held on February 2.

RESMIQ'S ACTIVITIES

ReSMiQ Networking meeting
Visit of the Concordia facilities, March 15th at 5:00 pm, Concordia University, EV building, room EV2.260.

More details

Message to members: we will be pleased to publish your news in forthcoming issues, let us know.

NEWS FROM OUR MEMBERS

EXPOSURE

Dr. Boukadoum from UQAM gave a keynote speech at the 3rd IEEE Latin American Symposium on CAS, in Mexico. More details

Dr. Sawan from Polytechnique gave a keynote speech at the SEMBA and BIOPRO, in Taiwan. More details

INVOLVEMENT

Dr. Tahar from Concordia University is the General Chair of the 30th edition of the ICCD conference, in Montréal. More details

Dr. Peter from Polytechnique is the TPC for the IEEE Optical MEMS and Nanophotonics 2012 conference, in Banff, Canada. More details

ACHIEVEMENT

Dr. Thibeault from ETS participated to the development of a technology used in testing aircraft electrical subsytems with Harness Scanner Inc. (THS) in St-Hubert. More details

Dr. Lakhssassi received a NSERC-I2I grant for the project "*Attentive Vision Technology for Object Detection in Multimodal Spatiotemporal imagery*".

NEWCAS 2012
10th IEEE International NEWCAS Conference
June 17 - 20, 2012, Montréal, Canada
www.newcas2012.org

SPOTLIGHT ON OTHER CONFERENCES

12th International Forum on Embedded MPSoC and Multicore (MPSoC'12), July 9 - 13, 2012, Québec, Canada. More details

55th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2012), August 5 - 8, 2012, Boise, Idaho, USA. More details

XXX IEEE International Conference on Computer Design (ICCD 2012), September 30 - October 3, 2012, Montréal, Canada. More details

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Visit our web site: www.resmiq.org

RESEARCH CONTRIBUTIONS

Some of the research achievements of our members.
This month, three major contributions are presented.

1. Safi-Harb, M.; Mirabbasi, S.; **Sawan, M**. A Time-Based Technique for Testing LC-Tank Oscillators, IEEE Transactions on Circuits and Systems—I: Regular Papers, On-line 2012.

This paper describes a new architecture that explores time-based signal-processing concepts for testing LC-tank radiofrequency (RF) oscillator circuits, and in particular, quadrature oscillators, while relying on low-frequency digital test equipment. The proposed system has two inputs that are two step-like signals with a time separation that is externally controlled. The output of the system is an amplified and digitized time separation that is a function of the time separation between the applied input steps and the oscillator output frequency characteristics. Coarse time digitization circuits are used to read the output, from which the frequency of oscillation of the oscillator is deduced. A proof-of concept circuit is designed and fabricated in a standard 0.18- m CMOS process. Experimental results confirm the feasibility of the proposed approach, which is demonstrated in this work with the successful on-chip measurement of 1.5 and 1.7 GHz oscillation frequencies.

2. Zhang, C.; **Wang, C.; Ahmad, M. O.** A Pipeline VLSI Architecture for Fast Computation of the 2-D Discrete Wavelet Transform, IEEE Transactions on Circuits and Systems—I: Regular Papers, On-line 2012.

In this paper, a scheme for the design of a high-speed pipeline VLSI architecture for the computation of the 2-D discrete wavelet transform (DWT) is proposed. The main focus in the development of the architecture is on providing a high operating frequency and a small number of clock cycles along with an efficient hardware utilization by maximizing the inter-stage and intra-stage computational parallelism for the pipeline. The inter-stage parallelism is enhanced by optimally mapping the computational task of multi decomposition levels to the stages of the pipeline and synchronizing their operations. The intra-stage parallelism is enhanced by dividing the 2-D filtering operation into four subtasks that can be performed independently in parallel and minimizing the delay of the critical path of bit-wise adder networks for performing the filtering operation. To validate the proposed scheme, a circuit is designed, simulated, and implemented in FPGA for the 2-D DWT computation. The results of the implementation show that the circuit is capable of operating with a maximum clock frequency of 134 MHz and processing 1022 frames of size 512$,times,$512 per second with this operating frequency. It is shown that the performance in terms of the processing speed of the architecture designed based on the proposed scheme is superior to those of the architectures designed using other existing schemes, and it has similar or lower hardware consumption.

3. Hoque, K.A.; **Ait-Mohamed, O.**; Abed, S. MDG–SAT: an automated methodology for efficient safety checking International, Journal of Critical Computer-Based Systems, vol. 3, no. 1–2, 2012.

Multiway decision graph (MDG) is a canonical representation of a subset of many–sorted first–order logic. It generalises the logic of equality with abstract types and uninterpreted function symbols. The area of satisfiability (SAT) has been the subject of intensive research in recent years, with significant theoretical and practical contributions. In this paper, we propose a new design verification tool integrating MDG and SAT, to check the safety of a design by invariant checking. Using MDG to encode the set of states provides a powerful mean of abstraction. We use a SAT solver to search for paths of reachable states violating the property under certain encoding constraints. In addition, we introduce an automated conversion–verification methodology to convert a directed formula (DF) into a conjunctive normal form (CNF) formula that can be fed to a SAT solver. The formal verification of this conversion is conducted within the HOL theorem prover. Finally, we present experimental results and a case study to show the correctness and the efficiency of our proposed methodology.

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